REMARKS

The Office Action dated February 8, 2005 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-33 are currently pending in the application and are respectfully submitted for consideration.

Claims 11-26 and 28-33 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In the Office Action, claims 1-10 and 27 were rejected under 35 U.S.C. §102(e) as being anticipated by Headrick (U.S. Patent No. 5,724,358). The rejection is respectfully traversed for the reasons which follow.

Claim 1, upon which claims 2-26 are dependent, recites a network switch comprising at least one port data port interface, a first memory, a second memory, and a memory management unit. The memory management unit is in connection with the at least one data port interface, the first memory, and the second memory. The memory management unit receives data from the at least one data port interface, determines if the data is to be stored in one of the first memory or the second memory, stores the data in one of the first memory or the second memory as a linked list, retrieves the data from one of the first memory or the second memory, and forwards the data for egress.

Claim 27, upon which claims 28-33 are dependent, recites a method for storing data in a network switch. The method includes the steps of receiving the data to be

transmitted to an egress at an input to a memory management unit, formatting the data received as a linked list, determining if the data is to be stored in a first memory or a second memory, and storing the data in the first memory or the second memory based on the determining step.

As will be discussed below, Headrick fails to disclose or suggest all of the elements of the claims, and therefore fails to provide the features discussed above.

Headrick discloses a high speed packet-switched digital switch that has a switch with a shared memory architecture. The switch may have a memory controller including an output queue for each output port. Each output queue includes a plurality of priority level sub-queues for routing data packets having different priority levels. The memory controller routes and buffers data packets on a per port, per priority level basis. The data packet has a header portion identifying one output port destination and a level of priority of the data within the packet. A buffer, shared by the output ports, stores the data packet in a selected buffer location based on the output port destination and priority level of the data packet. The data packets are output to the output ports in priority order.

Applicants respectfully submit that Headrick fails to disclose or suggest that the memory management unit determines if the data is to be stored in the first memory or the second memory and stores the data in the first memory or the second memory as a linked list, as recited in current claims 1 and 27. Headrick only discloses that "the first memory manager may process incoming ATM cells for ports 0-7, and the second memory manager may process incoming ATM cells for ports 8-15" (Headrick, Column 7, lines 1-

3. Headrick fails to disclose that the memory management unit determines which of the first memory or second memory the data is to be stored in. According to Headrick, incoming ATM cells for ports 0-7 are processed by a first memory manager, while incoming cells for ports 8-15 are processed by the second memory manager. Headrick does not disclose that any determination is made by the memory management unit with respect to within which memory the data should be stored. Therefore, Headrick fails to disclose at least this element of the claims.

Furthermore, Applicants respectfully assert that Headrick fails to disclose or suggest storing the data in the first memory or the second memory as a linked list. While Headrick does disclose the use of a linked list, it is not utilized within the first or second memory as recited in the present independent claims. In contrast, Headrick merely discloses that each output port has linked list in a pointer memory that forms an output queue for that output port so that the order that data packets are sent out of the port is known (Headrick, Column 7, lines 31-35). As such, Headrick fails to disclose that the memory management unit stores the data in the first or second memory as a linked list. Therefore, Applicants respectfully assert that Headrick also fails to disclose this element of the claims.

For at least the reasons discussed above, Applicants respectfully submit that Headrick fails to disclose or suggest all of the elements of claims 1 and 27. Thus, Applicants respectfully request that the rejection of the claims be withdrawn and that claims 1 and 27 be allowed.

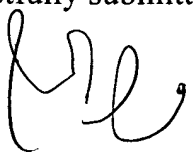
In addition, claims 2-10 are dependent upon claim 1. Therefore, claims 2-10 should also be allowed for at least their dependence upon claim 1, and for the specific limitations recited therein.

Applicants respectfully submit that Headrick fails to disclose or suggest critical and important elements of the claimed invention. These distinctions are more than sufficient to render the claimed invention unanticipated and unobvious. It is therefore respectfully requested that all of claims 1-33 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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